Assembly of Finite Element Methods on Graphics Processors

Cris Cecka Toru Takahashi Adrian Lew Eric Darve

Department of Mechanical Engineering Institute for Computational and Mathematical Engineering Stanford University

January 12th, 2011 Institute for Mathematics and its Applications





2 FEM Assembly

3 GPU Assembly

- LocalElem
- GlobalNZ
- SharedNZ
- Scatter and Reduction Arrays
- 4 Results
- **5** Application
- **6** Conclusion





- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations



- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations
- Productivity
 - Separate computational science from computer science



- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations
- Productivity
 - Separate computational science from computer science
- Portability



- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations
- Productivity
 - Separate computational science from computer science
- Portability
- Performance
 - Use domain knowledge and platform knowledge



- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations
- Productivity
 - Separate computational science from computer science
- Portability
- Performance
 - Use domain knowledge and platform knowledge
- Innovation
 - Change architectures and programming models under-the-hood



- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations
- Understands and uses topology
 - Domain decomposition
 - Sparsity pattern



- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations
- Understands and uses topology
 - Domain decomposition
 - Sparsity pattern
- Understands, transforms, and parallelizes loops
 - for(f <- faces(cell))
 for(c <- cell(mesh)) { ... }</pre>



- Liszt @ Stanford
 - Mesh-based PDEs on Heterogeneous Platforms
 - Analyzable DSL: Language with domain-specific features and restrictions that provide context for domain specific transformations
- Understands and uses topology
 - Domain decomposition
 - Sparsity pattern
- Understands, transforms, and parallelizes loops
 - for(f <- faces(cell))
 for(c <- cell(mesh)) { ... }</pre>
- Stencils statically analyzed from access patterns



- Sparse Linear Algebra coming of age on GPU.
 - Extensive research on Sparse Solvers on GPU.
 - Extensive research on SpMV.



- Sparse Linear Algebra coming of age on GPU.
 - Extensive research on Sparse Solvers on GPU.
 - Extensive research on SpMV.
- Non-linear and time-dependent problems require many assembly procedures.



- Sparse Linear Algebra coming of age on GPU.
 - Extensive research on Sparse Solvers on GPU.
 - Extensive research on SpMV.
- Non-linear and time-dependent problems require many assembly procedures.
- Want to use topology efficiently with a black-box element kernel.



- Sparse Linear Algebra coming of age on GPU.
 - Extensive research on Sparse Solvers on GPU.
 - Extensive research on SpMV.
- Non-linear and time-dependent problems require many assembly procedures.
- Want to use topology efficiently with a black-box element kernel.
- Can assemble, solve, update, and visualize on the GPU
 - Completely avoid transfers with CPU.
 - Fast (real-time) simulations with visualization.



FEM Direct Assembly

Most common FEM assembly procedure:

- Compute element data.
 - One by one.





Cecka, Takahashi, Lew, Darve

FEM Direct Assembly

Most common FEM assembly procedure:

- Compute element data.
 - One by one.
- Accumulate into global system.
 - Using a local index to global index mapping.





Nodal Data

















Two Key Choices:

Store Element Data In



Two Key Choices:

Store Element Data In

• Global Memory

Threads Assemble By

• Local Memory

Shared Memory



Two Key Choices:

Store Element Data In

• Global Memory

Computation / Assembly. Min computation.

Local Memory

• Shared Memory



Two Key Choices:

Store Element Data In

• Global Memory

Computation / Assembly. Min computation.

Local Memory

Fast read/write. No shared element data.

Shared Memory



Two Key Choices:

Store Element Data In

• Global Memory

Computation / Assembly. Min computation.

Local Memory

Fast read/write. No shared element data.

Shared Memory

Fast read/write. Small size.



Two Key Choices:

Store Element Data In

• Global Memory

Computation / Assembly. Min computation.

- Local Memory
 Fast read/write.
 No shared element data.
- Shared Memory

Fast read/write. Small size.

Threads Assemble By

Non-zero (NZ)

Row

Element



Two Key Choices:

Store Element Data In

• Global Memory

Computation / Assembly. Min computation.

Local Memory

Fast read/write. No shared element data.

• Shared Memory

Fast read/write. Small size.

Threads Assemble By

Non-zero (NZ)

Simple - Indexing. Imbalanced.

• Row

Element



Two Key Choices:

Store Element Data In

• Global Memory

Computation / Assembly. Min computation.

Local Memory

Fast read/write. No shared element data.

• Shared Memory

Fast read/write. Small size.

Threads Assemble By

Non-zero (NZ)

Simple - Indexing. Imbalanced.

• Row

More balanced. Lookup tables.

Element



Two Key Choices:

Store Element Data In

• Global Memory

Computation / Assembly. Min computation.

Local Memory

Fast read/write. No shared element data.

Shared Memory

Fast read/write. Small size.

Threads Assemble By

Non-zero (NZ)

Simple - Indexing. Imbalanced.

• Row

More balanced. Lookup tables.

 Element Race conditions.



• Assign one thread to one element.

- Compute the element data.
- Assemble directly into system.



• Assign one thread to one element.

- Compute the element data.
- Assemble directly into system.

Race conditions still possible!



Local-Element - Coloring the Mesh

• Assign one thread to one element.

- Compute the element data.
- Assemble directly into system.

Partition elements to resolve race conditions.

• Transform into a coloring problem.





Local-Element - Coloring the Mesh

• Assign one thread to one element.

- Compute the element data.
- Assemble directly into system.

Partition elements to resolve race conditions.

• Transform into a coloring problem.

Problems.

- No sharing of nodal or element data.
- Little utilization of GPU resources.





- Kernel1 Assign one thread to one element.
 - Compute the element data.
 - Store element data in global memory.



• Kernel1 - Assign one thread to one element.

- Compute the element data.
- Store element data in global memory.
- Kernel2 Assign one thread to one NZ.
 - Assemble from global memory.



Global-NZ

• Kernel1 - Assign one thread to one element.

- Compute the element data.
- Store element data in global memory.
- Kernel2 Assign one thread to one NZ.
 - Assemble from global memory.

Optimizing:

- Cluster the elements so they share nodes.
- Prefetch nodal data into shared memory.




Global-NZ

• Kernel1 - Assign one thread to one element.

- Compute the element data.
- Store element data in global memory.
- Kernel2 Assign one thread to one NZ.
 - Assemble from global memory.

Optimizing:

- Cluster the elements so they share nodes.
- Prefetch nodal data into shared memory.

Problems.

• Extra passes through global memory.





Global-NZ Data Flow

The optimized algorithm looks like:





- Assign one thread to one element.
 - Compute the element data.
 - Store element data in shared memory.



- Assign one thread to one element.
 - Compute the element data.
 - Store element data in shared memory.
- Reassign threads to NZs.
 - Assemble from shared memory.



- Assign one thread to one element.
 - Compute the element data.
 - Store element data in shared memory.
- Reassign threads to NZs.
 - Assemble from shared memory.

A set of NZs requires a set of elements.

• Must compute all "halo" element data.



- Assign one thread to one element.
 - Compute the element data.
 - Store element data in shared memory.
- Reassign threads to NZs.
 - Assemble from shared memory.
 - A set of NZs requires a set of elements.
 - Must compute all "halo" element data.
 - A set of elements requires a set of nodes.
 - Must gather all "halo" nodal data.



- Assign one thread to one element.
 - Compute the element data.
 - Store element data in shared memory.
- Reassign threads to NZs.
 - Assemble from shared memory.

A set of NZs requires a set of elements.

- Must compute all "halo" element data.
- A set of elements requires a set of nodes.
 - Must gather all "halo" nodal data.



- Assign one thread to one element.
 - Compute the element data.
 - Store element data in shared memory.
- Reassign threads to NZs.
 - Assemble from shared memory.

A set of NZs requires a set of elements.

- Must compute all "halo" element data.
- A set of elements requires a set of nodes.
 - Must gather all "halo" nodal data.

Problems.

• Shared memory size is very limiting.



Shared-NZ Data Flow

The optimized algorithm looks like:





Cecka, Takahashi, Lew, Darve

General procedure:

- Make a set of operations to be done for each partition.
- Pack these into an array such that reading is coalesced.



General procedure:

- Make a set of operations to be done for each partition.
- Pack these into an array such that reading is coalesced.

Scatter Array:





General procedure:

- Make a set of operations to be done for each partition.
- Pack these into an array such that reading is coalesced.

Scatter Array:



Reduction Array:





General procedure:

- Make a set of operations to be done for each partition.
- Pack these into an array such that reading is coalesced.

Scatter Array:



- Very fast.
- Highly adaptable.

Reduction Array:



- Significant setup cost.
- Significant memory cost.



Scaling with Element Number





Scaling with Element Order





GPU non-linear neoHookean model.







Cecka, Takahashi, Lew, Darve

GPU non-linear neoHookean model.

- Newton-Raphson update at each step.
- Assemble, solve, update, and render at each step.







GPU non-linear neoHookean model.

- Newton-Raphson update at each step.
- Assemble, solve, update, and render at each step.
- 28,796 Nodes. 125,127 Elements.







GPU non-linear neoHookean model.

- Newton-Raphson update at each step.
- Assemble, solve, update, and render at each step.
- 28,796 Nodes. 125,127 Elements.







Implementation





Improvement





Improvement





Improvement



Assembly Speed





Cecka, Takahashi, Lew, Darve

C. Cecka, A. Lew, E. Darve, Assembly of Finite Element Methods on Graphics Processors. IJNME, 2009.



C. Cecka, A. Lew, E. Darve, Assembly of Finite Element Methods on Graphics Processors. IJNME, 2009.

• Create and classify several GPU FEM assembly algorithms.



C. Cecka, A. Lew, E. Darve, Assembly of Finite Element Methods on Graphics Processors. IJNME, 2009.

- Create and classify several GPU FEM assembly algorithms.
- Identification of optimizations and limitations of each algorithm.



C. Cecka, A. Lew, E. Darve, Assembly of Finite Element Methods on Graphics Processors. IJNME, 2009.

- Create and classify several GPU FEM assembly algorithms.
- Identification of optimizations and limitations of each algorithm.
- Optimal method depends on the element:
 - Memory requirements of element kernels.
 - Computational requirements of element kernels.



C. Cecka, A. Lew, E. Darve, Assembly of Finite Element Methods on Graphics Processors. IJNME, 2009.

- Create and classify several GPU FEM assembly algorithms.
- Identification of optimizations and limitations of each algorithm.
- Optimal method depends on the element:
 - Memory requirements of element kernels.
 - Computational requirements of element kernels.
- Precomputation algorithms and support data structures.



C. Cecka, A. Lew, E. Darve, Assembly of Finite Element Methods on Graphics Processors. IJNME, 2009.

- Create and classify several GPU FEM assembly algorithms.
- Identification of optimizations and limitations of each algorithm.
- Optimal method depends on the element:
 - Memory requirements of element kernels.
 - Computational requirements of element kernels.
- Precomputation algorithms and support data structures.

C. Cecka, A. Lew, E. Darve. Application of Assembly, Solution, and Visualization of Finite Elements on Graphics Processors. GPU Gems. Preprint.

• Applying the methods to a high-performance FEM application.





- Know the structure and topology
- Leave the transfer matrix as arbitrary



- Know the structure and topology
- Leave the transfer matrix as arbitrary
- M2L stage:

$$\mathsf{L}(O) := \sum_{S \in \mathcal{I}(O)} \mathsf{D}^{(O,S)} \mathsf{M}(S)$$



- Know the structure and topology
- Leave the transfer matrix as arbitrary
- M2L stage:

$$L(O) := \sum_{S \in \mathcal{I}(O)} \mathbf{D}^{(O,S)} \mathbf{M}(S)$$

- 316 Transfer Matrices
- $|\mathcal{I}(O)| \leq 189$



FMM GPU Algorithms





Cecka, Takahashi, Lew, Darve

Basic Algorithm

Block = Observation Cell OThread = L_i


Block = Observation Cell OThread = L_i

For all $S \in \mathcal{I}(O)$



Block = Observation Cell OThread = L_i

```
For all S \in \mathcal{I}(O)
Read \mathbf{D}^{(S,O)}
Read \mathbf{M}(S)
```



Block = Observation Cell OThread = L_i

```
For all S \in \mathcal{I}(O)
Read \mathbf{D}^{(S,O)}
Read \mathbf{M}(S)
\mathbf{L}_{i} + = \mathbf{D}_{ij}^{(O,S)}\mathbf{M}_{j}(S)
Write \mathbf{L}_{i}
```



Block = Observation Cell OThread = L_i

```
For all S \in \mathcal{I}(O)
Read \mathbf{D}^{(S, O)}
Read \mathbf{M}(S)
\mathbf{L}_{i} + = \mathbf{D}_{ij}^{(O,S)}\mathbf{M}_{j}(S)
Write \mathbf{L}_{i}
```

		per observation cell
Read M-data	[word]	189 <i>r</i>
Read D-data	[word]	189 <i>r</i> ²
Write L-data	[word]	r
Operation counts	[flop]	189r(2r-1)
Flop-to-word ratio	[flop/word]	1.9 for $r = 32$ $(n = 4)$
		2.0 for $r = 256$ $(n = 8)$



Blocking Siblings









Cecka, Takahashi, Lew, Darve

Blocking Siblings



• Iterate over clusters instead of cells

		Per observation cluster	Per observation cell
Read M-data	[word]	8 · 26 · r	26 <i>r</i>
Read D-data	[word]	$26 \cdot 27 \cdot r^2$	$\frac{26 \cdot 27}{8} r^2$
Read/Write L-data	[word]	8 · 26 · r	26 <i>r</i>
Operation counts	[flop]	$8 \cdot 189 \cdot r(2r-1)$	189r(2r - 1)
Flop-to-word ratio	[flop/word]	4.2 for $r = 32$	
		4.3 for r = 256	



Cecka, Takahashi, Lew, Darve

Blocking Siblings



- Iterate over clusters instead of cells
 - Iterate over transfer class
 - Reuse the D matrix

		Per observation cluster	Per observation cell
Read M-data	[word]	8 · 26 · r	26 <i>r</i>
Read D-data	[word]	$26 \cdot 27 \cdot r^2$	$\frac{26 \cdot 27}{8} r^2$
Read/Write L-data	[word]	8 · 26 · r	26 <i>r</i>
Operation counts	[flop]	$8 \cdot 189 \cdot r(2r-1)$	189r(2r - 1)
Flop-to-word ratio	[flop/word]	4.2 for $r = 32$	
		4.3 for r = 256	



Cecka, Takahashi, Lew, Darve







- Parallel in the observation cell
- Iterate over *i* and *j* of the matrix





- Parallel in the observation cell
- Iterate over *i* and *j* of the matrix
 - Read sibling-equivalent M_i into shared memory (plus ghosts)
 - Read all 316 D_{ij} into shared memory





- Parallel in the observation cell
- Iterate over *i* and *j* of the matrix
 - Read sibling-equivalent M_i into shared memory (plus ghosts)
 - Read all 316 D_{ij} into shared memory





- Parallel in the observation cell
- Iterate over *i* and *j* of the matrix
 - Read sibling-equivalent M_i into shared memory (plus ghosts)
 - Read all 316 D_{ij} into shared memory
 - Perform the 189 interactions for each observation cell





- Parallel in the observation cell
- Iterate over *i* and *j* of the matrix
 - Read sibling-equivalent M_i into shared memory (plus ghosts)
 - Read all 316 D_{ij} into shared memory
 - Perform the 189 interactions for each observation cell
 - Can coalesce M_j reads
 - Can prevent shared memory bank conflicts





- Parallel in the observation cell
- Iterate over *i* and *j* of the matrix
 - Read sibling-equivalent M_j into shared memory (plus ghosts)
 - Read all 316 D_{ij} into shared memory
 - Perform the 189 interactions for each observation cell
 - Can coalesce M_j reads
 - Can prevent shared memory bank conflicts



		per chunk of size B	per observation cell
Read M-data	[word]	$(2B+4)^3 \cdot r \cdot P$	$\frac{(B+2)^3P}{B^3}r$
Read D-data	[word]	$316 \cdot r \cdot \frac{r}{P} \cdot P$	$\frac{316}{8B^3}r^2$
Read/Write L-data	[word]	$2 \cdot 8B^3 \cdot r \cdot \frac{r}{P} \cdot P$	2 <i>r</i> ²
Operation counts	[flop]	$8B^3 \cdot 189 \cdot \frac{r}{P}(2r-1) \cdot P$	189r(2r - 1)
Flop-to-word ratio	[flop/word]	108 for $r = 32$, $B = 4$, $P = 8$	
		133 for $r = 256$, $B = 4$, $P = 16$	

- Parallel in the observation cell
- Iterate over *i* and *j* of the matrix
 - Read sibling-equivalent M_i into shared memory (plus ghosts)
 - Read all 316 D_{ij} into shared memory
 - Perform the 189 interactions for each observation cell
 - Can coalesce *M_j* reads
 - Can prevent shared memory bank conflicts



FMM Performance





Cecka, Takahashi, Lew, Darve

FEM/FMM on GPU

27 / 28



• Domain specific language which is connectivity and platform aware.





- Domain specific language which is connectivity and platform aware.
- By providing a feature set and restrictions, it is analyzable.



- Domain specific language which is connectivity and platform aware.
- By providing a feature set and restrictions, it is analyzable.
- FEM assemblies on GPU which are connectivity aware and kernel independent.



- Domain specific language which is connectivity and platform aware.
- By providing a feature set and restrictions, it is analyzable.
- FEM assemblies on GPU which are connectivity aware and kernel independent.
- FMM M2L computations on GPU designed to address connectivity and remain kernel independent.

